**LAB 09**

**OBSERVATIONS / RESULTS & DISCUSSION:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Input: A** | **Input: B** | **(A●B)**  **7400**  **NAND** | **(A+B)**  **7402**  **NOR** | **A●B**  **7408**  **AND** | **A+B**  **7432**  **OR** |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | Not Connected | 1 | 1 | 0 | 0 |
| 1 | Not Connected | 1 | 0 | 0 | 1 |
| Not Connected | 0 | 1 | 1 | 0 | 0 |
| Not Connected | 1 | 1 | 0 | 0 | 1 |
| Not Connected | Not Connected | 0 | 1 | 0 | 0 |

**CONCLUSION:**

1. The output of AND Gate is only high when all inputs are high.

2. The output of OR Gate is low when all inputs are low.

3. The output of NOT Gate is inverse of input.

4. The output of NAND Gate is low when all inputs are high.

5. The output of NOR Gate is high when all inputs are low.

6. The output of XOR Gate is high when the inputs are at different logic levels.

7. The output of XNOR Gate is high when the inputs are at same logic levels.